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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/643,032	08/18/2003	John C. Pescatore	016295.1401	3223

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EXAMINER	
FAROOQ, MOHAMMAD O	

ART UNIT	PAPER NUMBER
2181	

DATE MAILED: 10/26/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/643,032	PESCATORE, JOHN C.	
	Examiner	Art Unit	
	Mohammad O. Farooq	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9 and 11-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9 and 11-23* is/are rejected.

7)☒ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The indicated allowability of claims 18-23 is withdrawn in view of the newly discovered reference(s). Rejections based on the newly cited reference(s) follow.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 2, 11, 12, 18 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicant admitted prior art in view of Garland et al. U.S. Pat. No. 6,389,120 B1.

3. As to claim 1, applicant admitted prior art teach system comprising:

a plurality of server modules (items 302a-n; fig. 3), each of said plurality of server modules having at least one central processing unit (CPU), memory and at least one server input-output (I/O) port (North Bridge having ports for plugging in the I/O module) background of the related technology; page 3 and Fig. 3); and

a plurality of input-output modules (I/O modules 1-m; fig. 3), each of said plurality of input-output modules having a module I/O port (background of the related technology; page 3; and fig. 3).

Applicant admitted prior art does not teach I/O switch having plurality of input buffers, plurality of output buffers, plurality of multiplexers and control logic for controlling plurality of multiplexer. Garland et al. teach I/O switch (item 200, fig. 2) having plurality of input buffers (memory in mux 202 would require multiple buffers to store data from multiple lines), plurality of output buffers (item 106, fig. 2), plurality of multiplexers (item 202, fig. 2) and control logic for controlling plurality of multiplexer (when the circuit for the switch in fig. 2 is repeated plurality of times, col. 3, lines 10-12; col. 3, line 34 – col. 4, line 14)). Therefore, it would have been obvious to one of ordinary skill in the art at the time to combine the teachings of applicant admitted prior art with Garland et al. because that would provide multiple telephone lines to provide multiple physical channels in data communication to provide high speed data communication (col. 1, lines 14-26 and 45-50).

4. As to claim 2, applicant admitted prior art teach a bridge (north bridge) for coupling the CPU to the memory and to the at least one server I/O port (disclosure in the background of the related technology; page 3 and Fig. 3).

5. As to claims 11 and 12, applicant admitted prior art teach server I/O port and module I/O port (fig. 3).

However, applicant admitted prior art does not teach input buffers, output buffers and mapping tables. Garland et al. teach input buffers, output buffers (item 120; fig. 2; col. 3, lines 1-13) and mapping tables (as it is common in the buffering mechanism). Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to combine the teachings of applicant admitted prior art with Garland et al. because that would provide multiple telephone lines to provide multiple physical channels in data communication (col. 1, lines 45-50).

6. As to claim 18, applicant admitted prior art teach system, comprising:

plurality of server I/O ports (items 302 a-n; fig. 3; background of the related technology; fig. 3); and

plurality of module I/O ports (North Bridge having ports for plugging in the I/O module, fig. 3; background of the related technology).

However, applicant admitted prior art does not teach I/O switch having plurality of input and output buffers, plurality of multiplexers and control logic for controlling plurality of multiplexers. Garland et al. teach I/O switch (item 200; fig. 2) having plurality of input buffers (memory in mux 202 would require multiple buffers to store data from multiple lines), plurality of output buffers (item 106; fig. 3), plurality of multiplexers (item 202, fig. 2) and control logic for controlling plurality of multiplexer (when the circuit for the switch in fig. 2 is repeated plurality of times, col. 3, lines 10-12; col. 3, line 34 – col. 4, line 14)). Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to combine applicant admitted prior art with Garland et al. because that would provide multiple telephone lines to provide multiple physical channels in data communication to (col. 1, lines 45-50).

7. Claim 19 has similar limitation as claim 12. Applicant admitted prior art and Garland et al. in combination teach apparatus as set forth in claim 12. Therefore, Applicant admitted prior art and Garland et al. in combination also teach apparatus as set forth in claim 19.

8. Claims 3 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicant admitted prior art in view of Garland et al. U.S. Pat. No. 6,389,120 B1 further in view of Futral, U.S. Pat. No. 6,112,263

9. As to claim 3, neither applicant admitted prior art nor Garland et al. teach system, further comprising at least one native input-output device in at least one of said plurality of server modules. Futral teaches system, further comprising at least one native input-output device (IOPs, items 236 and 238; fig. 2a) in at least one of said plurality of server modules. Therefore, it would have been obvious to one of ordinary skill in the art at the time of teaching to modify the combination of applicant admitted prior art and Garland et al. with Futral because that would provide different platforms with their own instance of an operating system to access to the same I/O device (col. 1, lines 40-45).

10. As to claim 4, neither applicant admitted prior art nor Garland et al. teach wherein the at least one native I/O device is selected from the group consisting of USB, serial, keyboard, video and mouse. Futral teaches system, wherein the at least one native I/O device is selected from the group consisting of USB, serial, keyboard, video and mouse (i.e. hardware elements such as connectors and cables; col. 5, line 62- col. 6, line 21). Therefore, it would have been obvious to one of ordinary skill in the art at the time of teaching to modify the combination of applicant admitted prior art and Garland et al. with Futral because that would provide different platforms with their own instance of an operating system to access to the same I/O device (col. 1, lines 40-45).

11. Claims 5 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicant admitted prior art in view of Garland et al. U.S. Pat. No. 6,389,120 B1 further in view of Casey, U.S. 2003/0142674 A1.

12. As to claim 5, neither applicant admitted prior art nor Garland et al. teach Ethernet controller. Casey teaches Ethernet controller (inherent; paragraph 0002). However, it would have been obvious to one of ordinary skill in the art at the time of invention to modify the combination of applicant admitted prior art and Garland with Casey because that would provide label values to the VPLS service (abstract).

13. As to claim 17, neither applicant admitted prior art nor Garland et al. teach user interface.

Casey teaches user interface (inherent because of CE; paragraph 0023). Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to modify the combination of applicant admitted prior art and Garland et al. with Casey because that would provide label values to the VPLS service (abstract).

14. Claims 6-9 and 20-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicant admitted prior art in view of Garland et al. U.S. Pat. No. 6,389,120 B1 further in view of Casey, US 2003/142674 A1 and Futral, U.S. Pat. No. 6,112,263.

15. As to claims 6-9, neither applicant admitted prior art nor Garland et al. and Casey teach a serial port, server I/O port is a serial port, server I/O port is a serial PCI I/O port and module I/O port is a serial PCI I/O port. Futral teaches system, wherein module I/O port is a serial port, server I/O port is a serial port, server I/O port is a serial PCI I/O port and module I/O port is a serial PCI I/O port (col. 6, lines 3-48). Therefore, it would have been obvious to one of ordinary skill in the art at the time of teaching to modify the combination of applicant admitted prior art, and Garland et al. and Casey with Futral because that would provide different platforms with their own instance of an operating system to access to the same I/O device (col. 1, lines 40-45).

16. Claims 20-23 have similar limitations as claims 6-9. Applicant admitted prior art, Garland et al., Casey and Futral in combination teach apparatus as set forth in claims 6-9. Therefore, Applicant admitted prior art, Garland et al., Casey and Futral in combination also teach apparatus as set forth in claims 20-23.

17. Claims 13-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicant admitted prior art in view of Garland et al. U.S. Pat. No. 6,389,120 B1 further in view of Swoboda et al. U.S. Pat. No. 6,032,268.

18. As to claims 13-16, neither applicant admitted prior art nor Garland et al. teach initialization logic, initialization logic is external, low pin count interface and wherein low pin count interface is from consisting I2C and JTAG. Swoboda et al. teach initialization logic, initialization logic is external (reset; col. 19, lines 17-22), low pin count interface (and wherein low pin count interface is from consisting I2C (as I2C is very common in the art) and JTAG (col. 15, lines 50-61). Therefore, it would be obvious to one of ordinary skill in the art at the time of invention to modify the combination of applicant admitted prior art and Garland et al. with Swoboda et al. because that would provide re-useable tests for related chips and systems (col. 3, lines 1-24).

Response to Arguments

19. Applicant's arguments with respect to claims 1-9 and 11-23 have been considered but are moot in view of the new ground(s) of rejection.

20. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mohammad O. Farooq whose telephone number is (571) 272-4144. The examiner can normally be reached on 9:00am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dov Popovici can be reached on (571) 272-4083. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mohammad O. Farooq
October 7, 2005

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